SHARP

LM10V332

Color STN LCD Module

(Model Number: LM10V332)

Specifications

Spec No.: LC99213A

Dated: May 31. 2002

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SPECIFICATION

DEVICE SPECIFICATION for
Passive Matrix Color LCD Module
(640×480 dots)

Model No.

LM10V332

☐CUSTOMER'S APPROVAL

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BY _____

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SHARP CORPORATION

SHARP

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DATE	REF.PAGE PARAGRAPH DRAWING No.	REVISED NO.	SUMMARY	CHECK AND APPROVAL
JUL.12.1999	P5,P6	△1	Ambient temperature	
	P5 /Table5	△1	Supply current, Power comsumption, Rush current	
	P10 /Table7	△1	Data set up time	
	P16 /Fig7	△1		
	P21 /Fig11	△1	VDD on/off cycle, Regulation “d”,”g”,”h”	
	P25	△1	Applicable inspection standard	

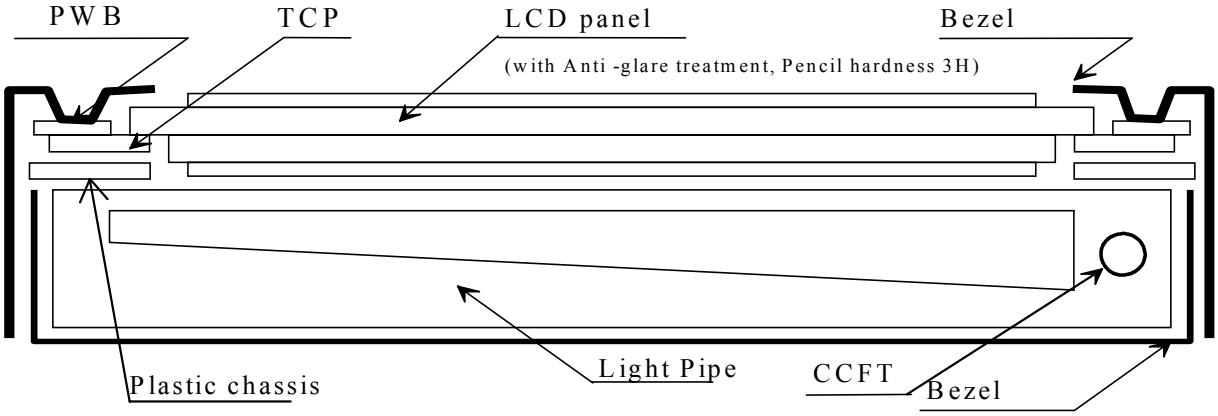
● Contents Page

1. Application

This data sheet is to introduce the specification of LM10V332, Passive Matrix type Color LCD module.

2. Construction and Outline

Construction: 640×480 dots color display module consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto, TCP(tape carrier package) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT back light and bezel to fix them mechanically.
Signal ground(Vss) is connected with the metal bezel.
DC/DC converter is built in.



Outline :See Fig. 13
Connection :See Fig. 13 and Table 6

3. Mechanical Specification

Table1

Parameter	Specifications	Unit
Outline dimensions	264±0.5(W)×193.6±0.5(H)×8.5MAX(D)	Mm
Bezel opening area	215.2±0.3(W)×162.4±0.3(H)	mm
Display format	640(W)×480(H) full dots	mm
Dot size	0.09×RGB(W)×0.31(H)	—
Dot spacing	0.02	mm
*1 Base color	Normally black *2	—
Weight	Approx. 450	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*2 Negative-type display

Display data "H" : ON → transmission

Display data "L" : OFF → light isolation

4.Absolute Maximum Ratings

4-1.Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage(Logic)	V_{DD}-V_{SS}	0	6.0	V	Ta=25 ℃
Input voltage	V_{IN}	-0.3	V_{DD}+0.3	V	Ta=25 ℃

4-2.Environment Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-25 ℃	+60 ℃	0 ℃	⚠1 ~~+50~~ ℃ +40℃	Note 4)
Humidity	Note 1)		Note 1)		No condensation
Vibration	Note 2)		Note 2)		3 directions(X/Y/Z)
Shock	Note 3)		Note 3)		6 directions(±X±Y±Z)

Note 1) Ta≦40 ℃ 95 % RH Max.

Ta＞40 ℃ Absolute humidity shall be less than Ta=40 ℃/95 % RH.

Note 2)

Table 4

Frequency	10 Hz～57 Hz	57 Hz～500 Hz
Vibration level	-	9.8 m/s^2
Vibration width	0.075 mm	-
Interval	10 Hz～500 Hz～10 Hz/11.0 min	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Acceleration : 490 m/s^2

Pulse width : 11 ms

3 times for each directions of ±X/±Y/±Z

Note 4) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25℃ and it becomes stable.

5.Electrical Specifications

5-1. Electrical charasteristics

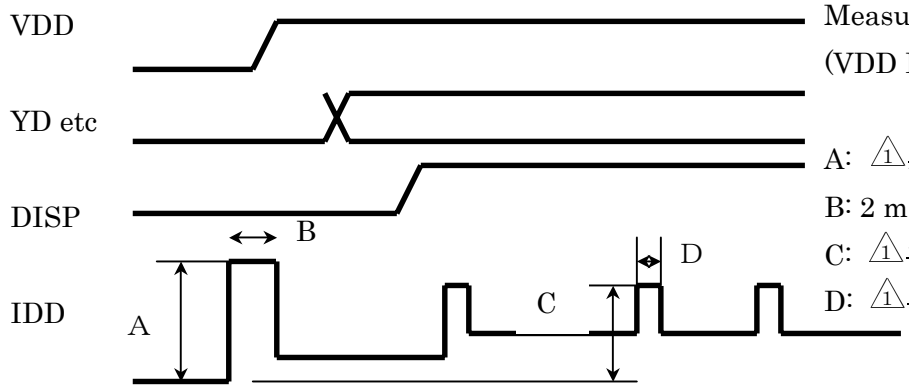
Table 5 Ta=25 ℃ VDD= 5.0 V±10 %

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}	⚠1Ta = 0～~~50~~ 40℃(Note 1)		4.5	5.0	5.5	V
Contrast adjust voltage	Vcon -V_{SS}	⚠1Ta = 0～40 ℃		0.8	1.95	2.8	V
Input signal voltage	V_{IN}	"H" level	⚠1Ta = 0～~~50~~ 40℃	0.8V_{DD}	－	V_{DD}	V
		"L" level		0	－	0.2V_{DD}	V
Supply current(Logic)	I_{DD}	Note 2)		－	⚠1~~210~~ 90	⚠1~~320~~ 135	mA
Power comsumption	Pd	Note 2)		－	⚠1~~1050~~ 450	⚠1~~1600~~ 680	mW
Rush current(Logic)	I_{DD}	Ta=25℃,Note 1)-①		－	－	⚠1~~2A×2~~ 1A×2	ms
		Ta=25℃,Note 1)-②		－	－	⚠1~~1A×10~~ 0.5A×20	μs

Note 1) Under the following conditions.;Logic voltage(VDD) should be designed to supply following Inrush current.

①Immediately after the rise of V_{DD} .

②Under the situation that DISP signal is on and kept steady.



Measurement Circuit: TMD-18-3 (VDD Power Supply)(TAKASAGO)

A: ⚠1~~2 A~~ 1AMAX

B: 2 ms MAX

C: ⚠1~~1 A~~ 0.5AMAX

D: ⚠1~~10 μs~~ 20 μs MAX

Note 2) Under the following condetions

Vcon-Vss: contrast max.(1.95V typ.)

VDD-VSS=5V,Frame frequency=120Hz, Display pattern : black/white stripe pattern.

□□□□□□□□□□□□□□□□□□□□

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■■■■■■■■■■■■■■■■■■■■

This value Is direct current.

5-2.Interface signals

● LCD

Table 6

Pin No.	Symbol	Description	Level
1	DL4	Display data signal	H(ON), L(OFF)
2	VSS	Ground potential	-
3	DL5	Display data signal	H(ON), L(OFF)
4	YD	Scan start-up signal	"H"
5	DL6	Display data signal	H(ON), L(OFF)
6	LP	Input data latch signal	"H" → "L"
7	DL7	Display data signal	H(ON), L(OFF)
8	VSS	Ground potential	-
9	VSS	Ground potential	-
10	XCK	Data input clock signal	"H" → "L"
11	DL0	Display data signal	H(ON), L(OFF)
12	Vcon	Contrast adjust voltage	-
13	DL1	Display data signal	H(ON), L(OFF)
14	VDD	Power supply for logic and LCD	-
15	VSS	Ground potential	-
16	VDD	Power supply for logic and LCD	-
17	DL2	Display data signal	H(ON), L(OFF)
18	DISP	Display control signal	H(ON), L(OFF)
19	DL3	Display data signal	H(ON), L(OFF)
20	NC	-	-
21	VSS	Ground potential	-
22	DU3	Display data signal	H(ON), L(OFF)
23	DU4	Display data signal	H(ON), L(OFF)
24	DU2	Display data signal	H(ON), L(OFF)
25	DU5	Display data signal	H(ON), L(OFF)
26	DU1	Display data signal	H(ON), L(OFF)
27	VSS	Ground potential	-
28	DU0	Display data signal	H(ON), L(OFF)
29	DU6	Display data signal	H(ON), L(OFF)
30	VSS	Ground potential	-
31	DU7	Display data signal	H(ON), L(OFF)

● CCFT

Pin No	Symbol	Description	Level
1	HV	High voltage line (from Inverter)	-
2	NC	NC	-
3	GND	Ground line (from Inverter)	-

● LCD

Used connector ：DF9B-31P-1V(HIROSE)

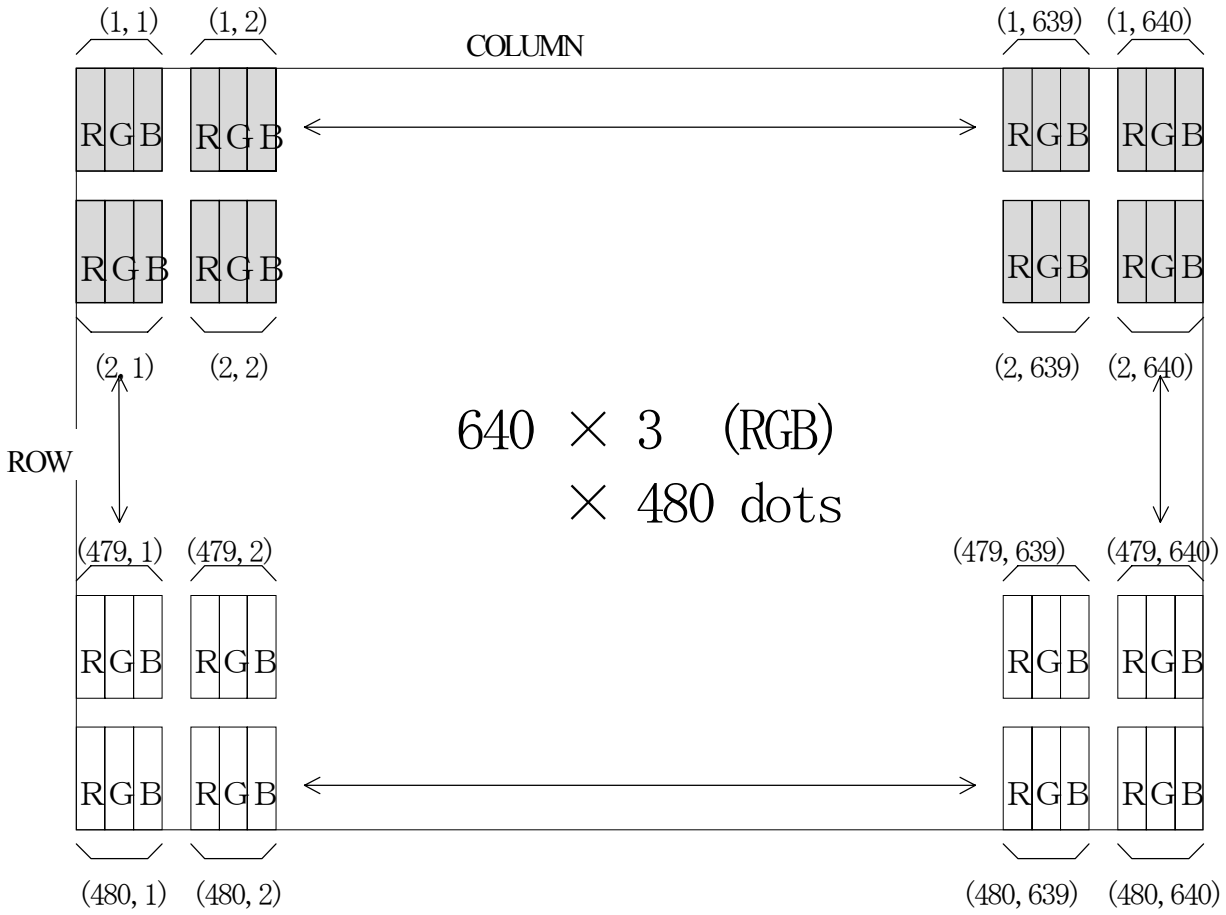
Mating connector：DF9B-31S-1V(HIROSE)

● CCFT

Used connector ：BHR-03VS-1(JST)

Mating connector：SM02(8.0)B-BHS(JST)

Except above connector shall be out of guaranty.



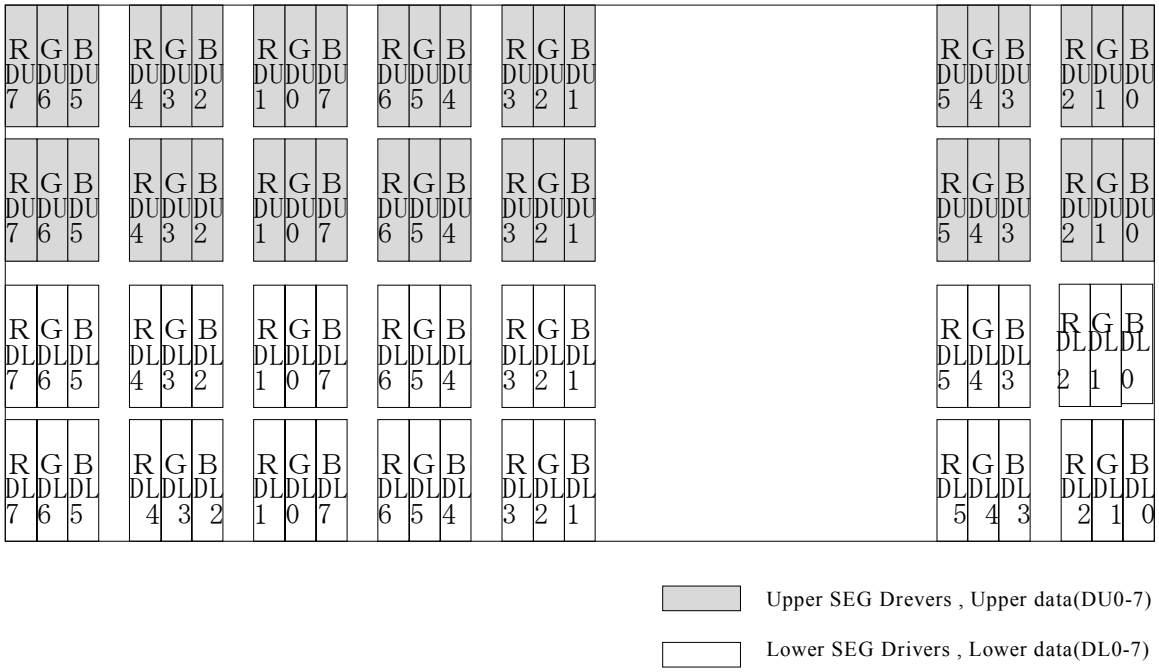


Fig.1 Dot chart of display area

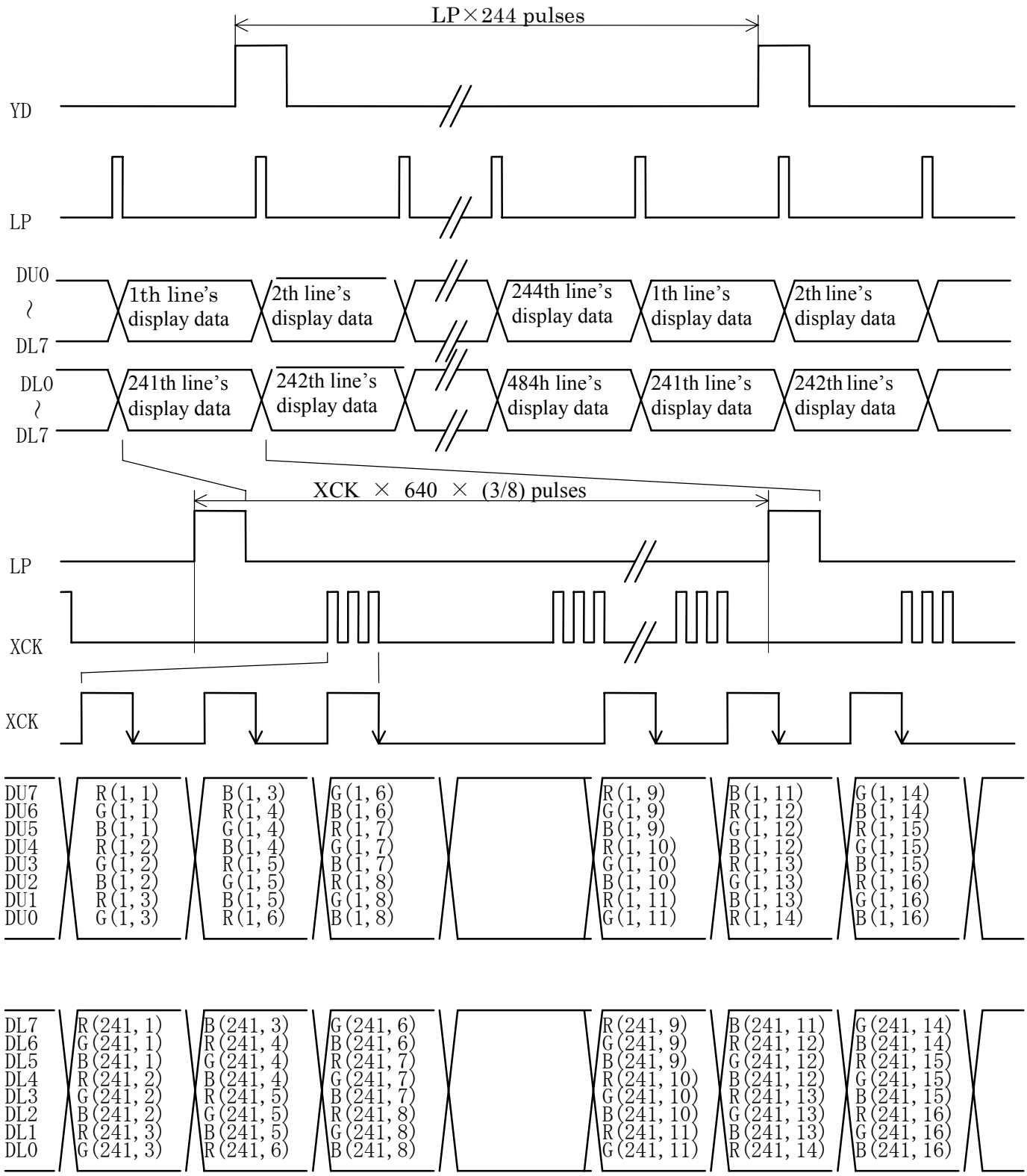


Fig.2 Data Input timing chart

Table 7 Interface timing ratings

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle *1	t_{FRM}	8.33		16.94	ms
YD signal "H" level set up time	t_{HYS}	100			ns
"H" level hold time	t_{HYH}	100			ns
"L" level set up time	t_{LYS}	100			ns
"L" level hold time	t_{LYH}	40			ns
LP signal "H" level pulse width	t_{WLPH}	200			ns
XCK signal clock cycle	t_{CK}	80			ns
"H" level clock width	t_{WCKH}	30			ns
"L" level clock width	t_{WCKL}	30			ns
Data set up time	t_{DS}	△1 ~~5~~ 15			ns
hold time	t_{DH}	40			ns
LP ↑ allowance time from XCK ↓	t_{LS}	200			ns
XCK ↑ allowance time from LP ↓	t_{LH}	200			ns
Input signal rise/fall time *1	t_r,t_f			12	ns

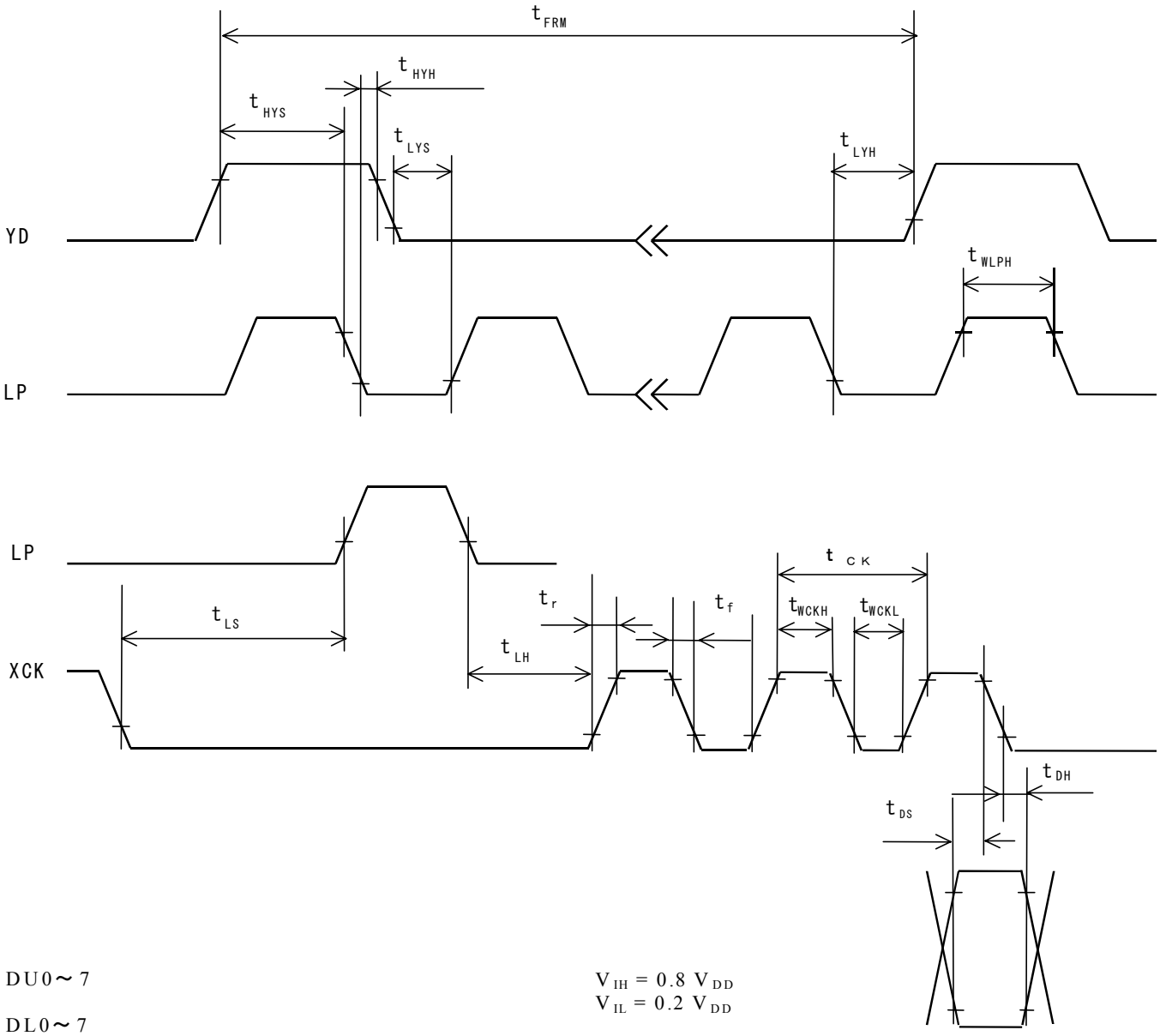
*1 LCD module functions at the minimum frame cycle of 8.33 ms(Maximum frame frequency of 120 Hz).

Owing to the characteristics of LCD module, "shadowing" will become more eminent as frame frequency goesup, while flicker will be reduced.

According to our experiments, frame cycle of 8.33 ms Min. or frame frequency of 120 Hz Max. will demonstrate optimum display quality in terms of flicker and "shadowing". But since judgment of display quality is subjective and display quality such as "shadowing" is pattern dependent, it is recommended that decision of frame frequency, to which power consumption of the LCD module is proportional, be made based on your own through testing on the LCD module with every possible patterns displayed on it.

The intervals of one LP fall and next must be always the same, and LPs must be input continuously.

The intervals must be 70 μ s Max.



DU0～7

DL0～7

$V_{IH} = 0.8\ V_{DD}$
$V_{IL} = 0.2\ V_{DD}$

Fig.3 Interface timing chart

6. Module Driving Method

6-1. Circuit configuration

Fig.9 shows the block diagram of the module's circuitry.

6-2. Display face configuration

The display consists of 640×3(R,G,B)×480 dots as shown in Fig. 1.

The interface is single panel with double drive to be driven at 1/240(1/244) duty ratio.

(1/240:an odd number frame, 1/244:an even number frame)

6-3. Input data and control signal

The LCD driver is 240 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (640×3 R,G,B) will be sequentially transferred in the form of 8 bit parallel data through shift registers from top left of the display together with clock signal (XCK).

When input of one row (640×3 R,G,B) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP) then,the corresponding drive signals will be transmitted to the 640×3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered. When data for 640×3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 240(244)th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.

Simultaneously the same scanning sequence occur at the lower panel.
Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive wave-form shall be inverted at every display frame to prevent the generation of such DC voltage. Control signal M plays such a role.

Because of the characteristics of CMOS driver LSI, the power consumption of the display module goes up with the clock frequency of XCK.
To minimize data transfer speed of XCK clock the LSI has the system of transferring 8 bit parallel data through the 8 lines of shift registers.
Thanks to this system the power consumption of the display module is minimized.

In this circuit configuration, 8 bit display data shall input to data input pins of DU0-7 and DL0-7.

Furthermore, the display module has bus line system for data input to minimize the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI right next side is selected when data of 240 dot (30XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face. This process is followed simultaneously both at the top and bottom column drivers LSI's.

Thus data input will be made through 8 bit bus line sequentially from the left end of the display face.

Since this display module contains no refresh RAM, it requires the above data and timing pulse inputs even for static display.

The timing chart of input signals are shown in fig. 3 and Table 7.

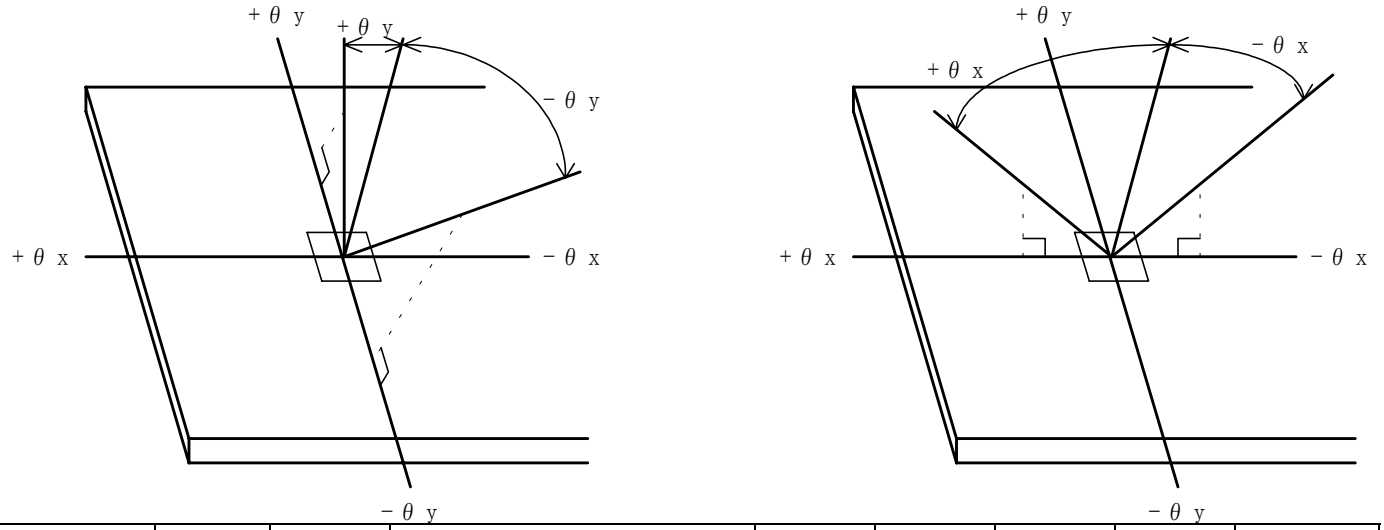
7. Optical Characteristics

Following spec are based upon the electrical measuring conditions, on which the contrast of perpendicular direction($\theta x = \theta y = 0^\circ$) will be MAX..

Ta=25℃,VDD=5.0V,VCON-VSS=Vmax

Table 8

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx	Co>5.0	$\theta y = 0^\circ$	-30	—	30	deg.	Note 1)
		θy		$\theta x = 0^\circ$	-15	—	25	deg.	
Contrast ratio		Co	$\theta x = \theta y = 0^\circ$		35	50	—	—	Note2)
Response time	Rise	τr	$\theta x = \theta y = 0^\circ$		—	220	300	ms	Note3)
	Decay	τd	$\theta x = \theta y = 0^\circ$		—	80	100	ms	
		x	$\theta x = \theta y = 0^\circ$		—	0.275	—	—	



		y	$\theta x = \theta y = 0^\circ$		—	0.320	—	—	

Fig.4 Definition of Viewing Angle

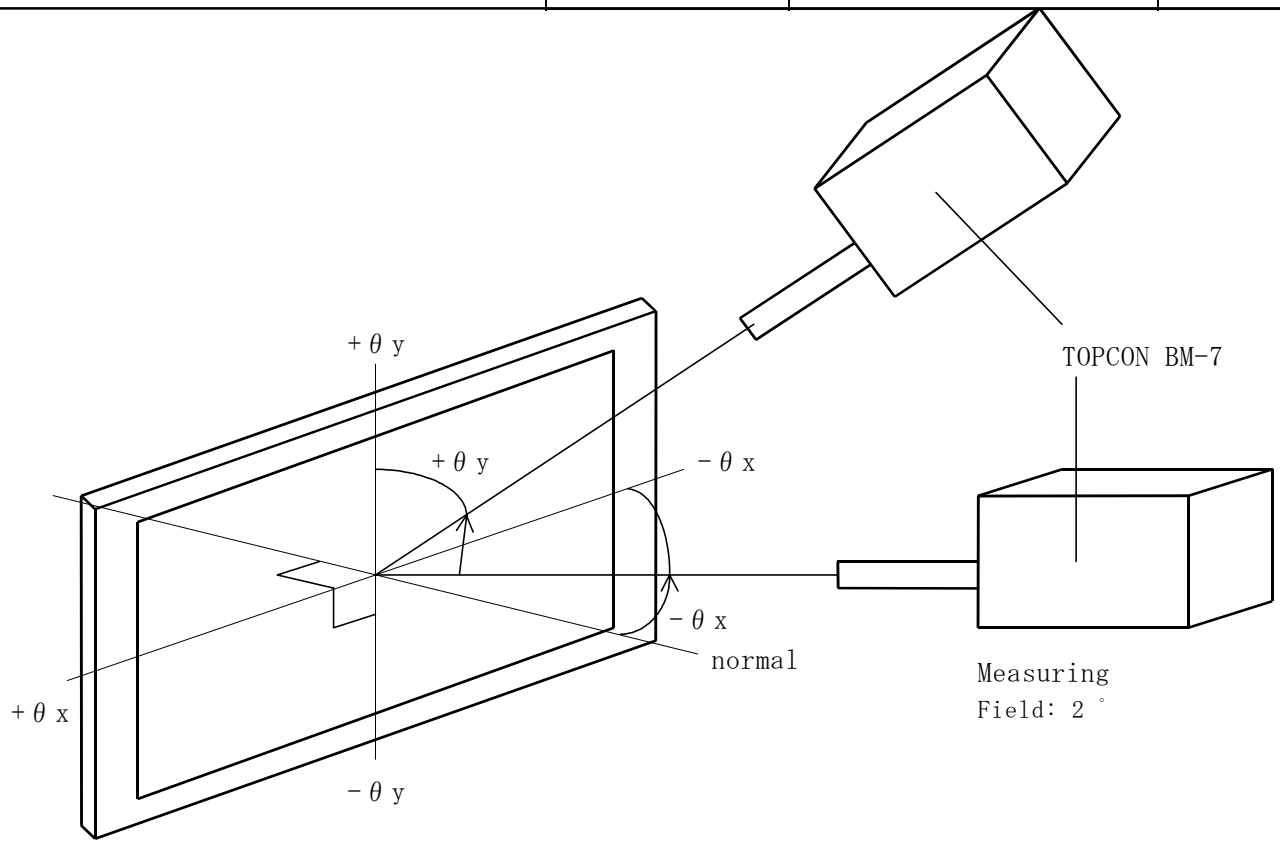
Note 1) The viewing angle range is defined as shown Fig.4.

Note 2) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixes "White" at Vmax}}{\text{Luminance(brightness) all pixes "dark " at Vmax}}$$

Vmax is defined in Fig.6.

Note 3) The response characteristics of photo-detector output are measured as shown in Fig.7, assuming that input signals are applied so as to select and deselect the dot to be measured, in the optical characteristics test method shown in Fig.5.



Measuring Spot Size : ϕ 10 mm

θ x : Angle from “normal” to viewing surface rotated about the horizontal axis.

θ y : Angle from “normal” to viewing surface rotated about the vertical axis.

Fig.5 Optical Characteristics Test Method I

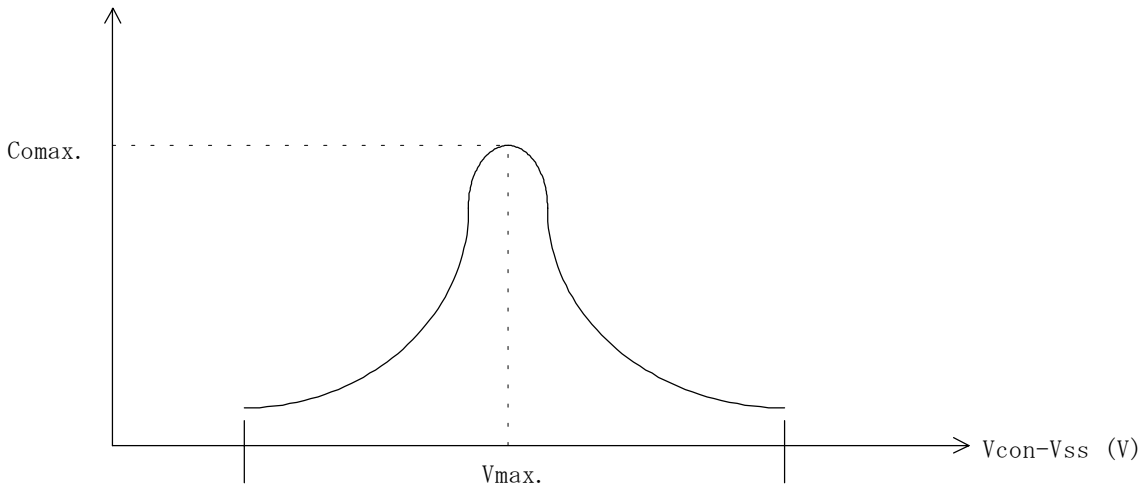
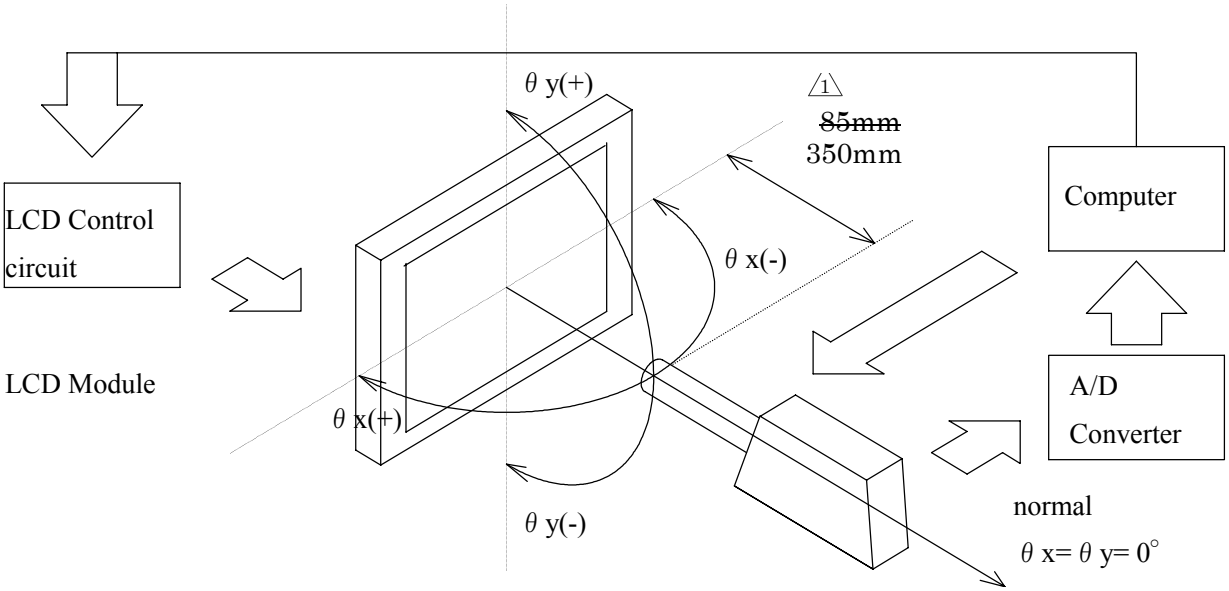


Fig.6 Definition of Vmax

(Response Measurement)

Ta = 25 ℃

In dark room



△1

TOPCON BM7 ~~+ quartz fiber~~

(Measuring spot size : ϕ 10 mm, Measuring Field : 2°)

Fig. 7 Optical Characteristics Test Method Ⅱ

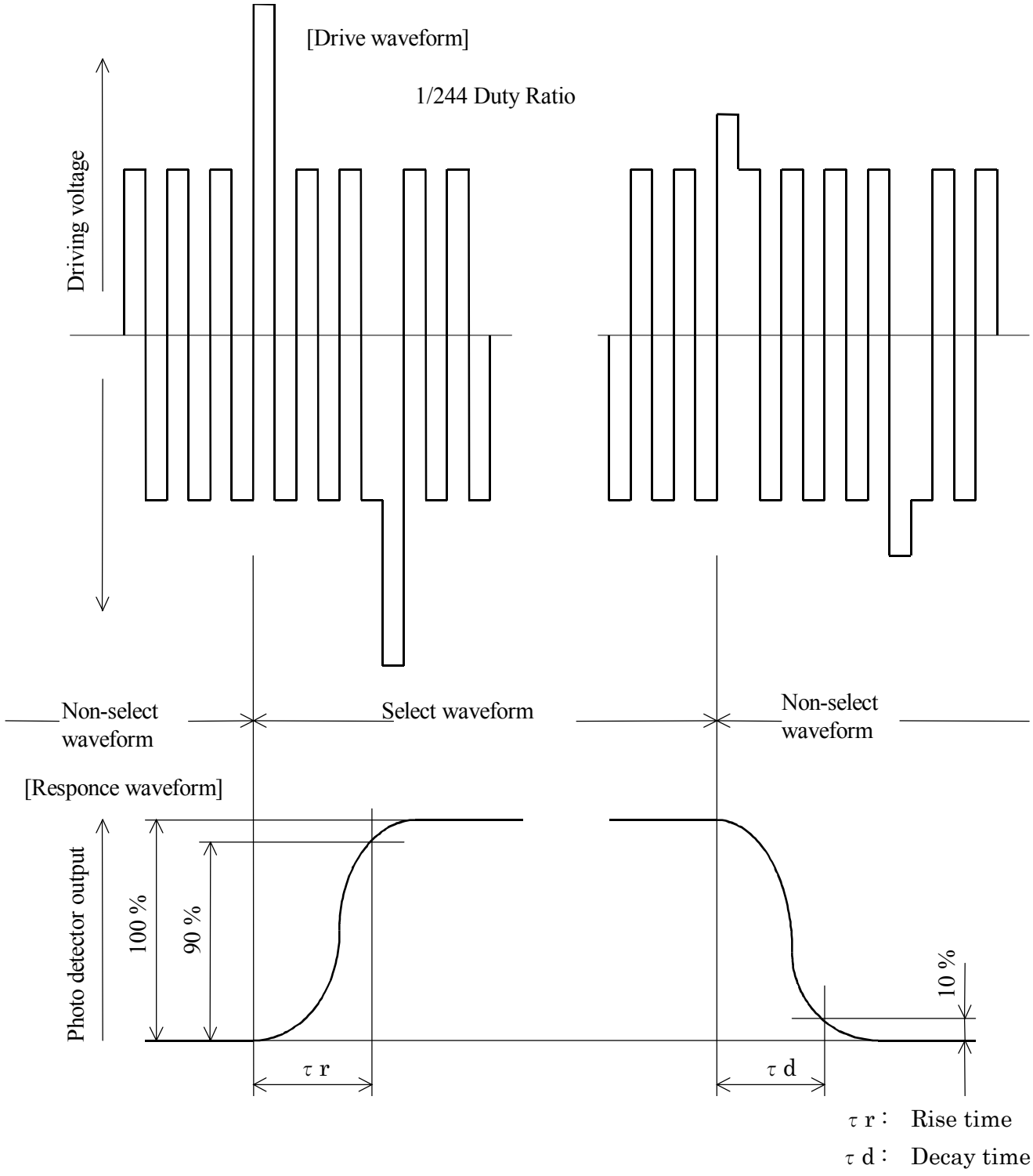


Fig.8 Definition of Response time

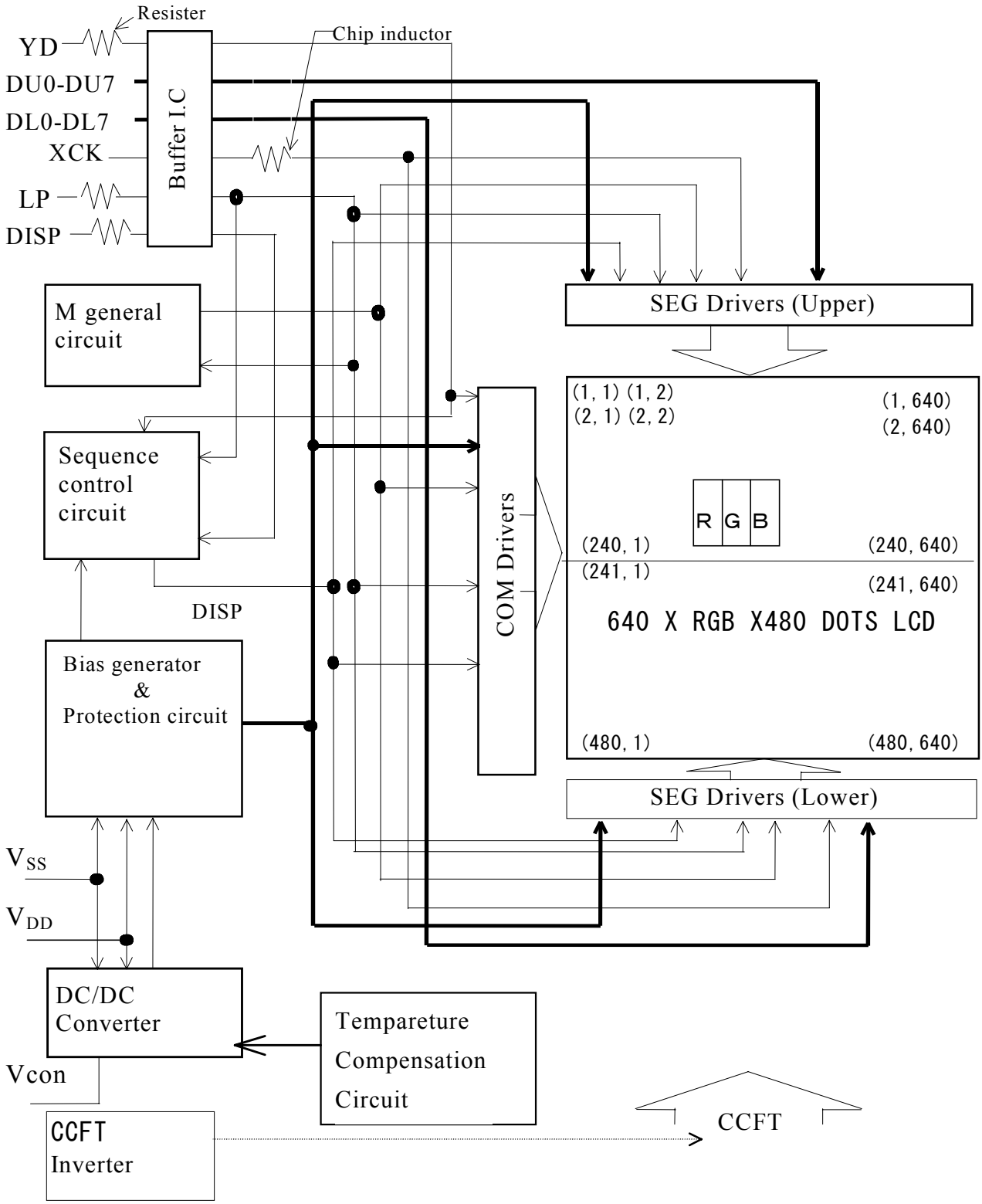


Fig. 9 Circuit block diagram

8.Characteristics of Backlight

The ratings are given on condition that the following conditions are satisfied.

1) Rating(Note)

Parameter	MIN.	TYP.	MAX.	Unit
Brightness	120	160	—	cd/m^2

2) Measurement circuit : CXA-M10L(TDK) (at IL = 5.5 mArms)

3) Measurement equipment : BM-7 (TOPCON Corporation)

4) Measurement conditions

4-1. Measurement circuit voltage : DC = 10.6 V, at primary side

4-2. LCD: All digits WHITE, VDD= 5 V, Vcon-VSS = Vmax,
DU0-7="H"(White), DL0-7="H"(White)

4-3. Ambient temperature : 25 ℃

Measurement shall be executed 30 minutes after turning on.

5) Used lamp : K-CE235-24-50BH(WEST ELECTRIC CO.,LTD.) : 1 pc

5-1) Rating (1pc)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Lamp voltage	V_L	—	520	—	Vrms	—
Lamp current	I_L	—	5.5	—	mArms	(*1)
Lamp power consumption	P_L	—	2.86	—	W	(*2)
Lamp frequency	F_L	30	—	70	kHz	—
Kick-off voltage	V_S	—	—	760	Vrms	Ta=25 ℃
		—	—	1300	Vrms	Ta= 0 ℃(*3)
Lamp life time	L_L	25 000	40 000	—	h	Ta=25 ℃(*4)
	L_L	1 000	—	—	h	Ta=0 ℃(*4)

Within no conductor closed. (CCFT only)

*1 It is recommended that IL be not more than 5.5mArms so that heat radiation of CCFT backlight may least affect the display quality.

*2 Power consumption excluded inverter loss.

*3 The circuit voltage(VS) of the inverter should be designed to have some margin, because VS may be increased due to the leak current in case of the LCD module.

*4 Average life time of CCFT will be decreased when LCD is operating at lower temperature.

5-2) Operating life

The operating life time is 25 000 hours or more at 5.5 mA , at 25℃.

(Operating life with CXA-M10L or equivalent.)

The inverter should meet the following conditions to keep the specified life time of used lamp;

Since, symmetric waveform without spike in positive and negative

Output frequency range ： 30 kHz-70 kHz

Make sure the operating conditions by executing the burn-in enough time.

The operating life time is defined as having ended when any of the following conditions occur;

25± 1 ℃

When the voltage required for initial discharge has reached 110 % of the initials value.

When the illuminence quantity of light has decreased to 50 % of the initials value.

(NOTE) Rating are defined as the average brightness inside the viewing area specified in Fig.10.

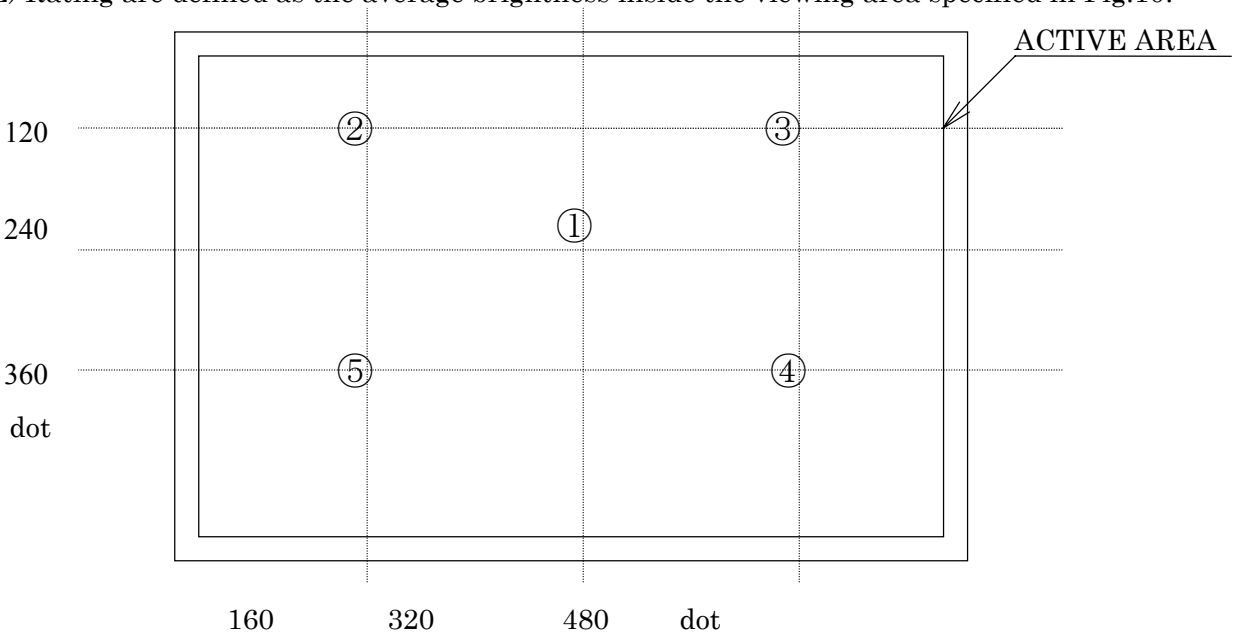


Fig.10 Measuring points (①－⑤)

9. Supply voltage sequence condition

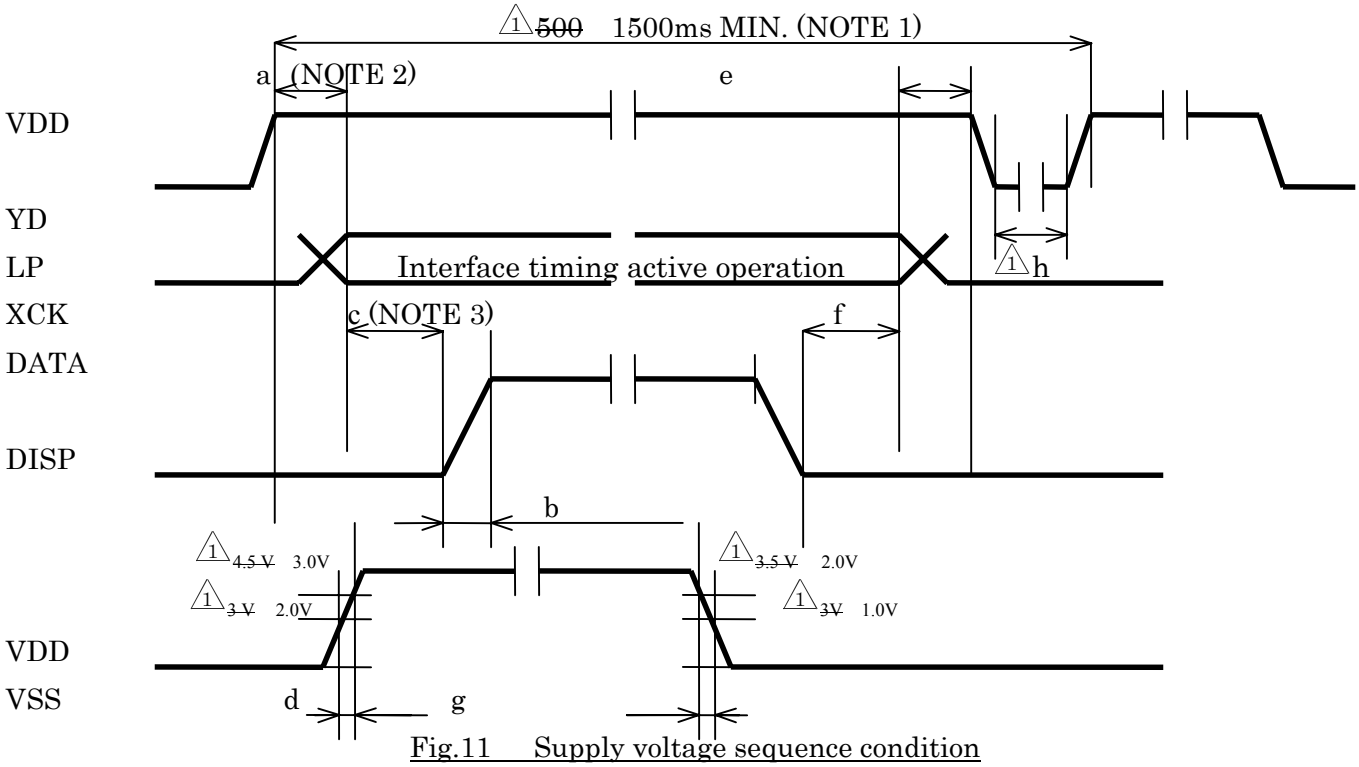


Fig.11 Supply voltage sequence condition

	POWER ON	
Symbol	Allowable value	
a	0 ms MIN.	1 s MAX.
b	—	100 ns MAX.
c	50 ms MIN.	-
d	-	10 ms MAX.

	POWER OFF	
Symbol	Allowable value	
e	0 ms MIN.	1 s MAX.
f	0 ms MIN.	1 s MAX.
g	△1 ~~10 ms MIN.~~ 1 ms MIN.	—
△1 h	1s MIN.	—

(NOTE 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

(NOTE 2) In this period, YD and LP shall be "L" level.

(NOTE 3) Before DISP rise up, the signals of YD,LP,XCK,DATA must be input, and the above condition of "a" must be satisfied. The signals which comply with the interface timing in Fig.2,Fig.3, and table 7, must be input.

10. Cautions

1) Industrial(Mechanical) design of the product in which this LCD module will be incorporated must be made so that the viewing angle characteristics of the LCD may be optimized.

This module's viewing angle is illustrated in Fig.12.

θ y MIN. < viewing angle < θ y MAX.

(For the specific values of θ y MIN., and θ y MAX., refer to the table8)

Please consider the optimum viewing conditions according to the purpose when installing the module.

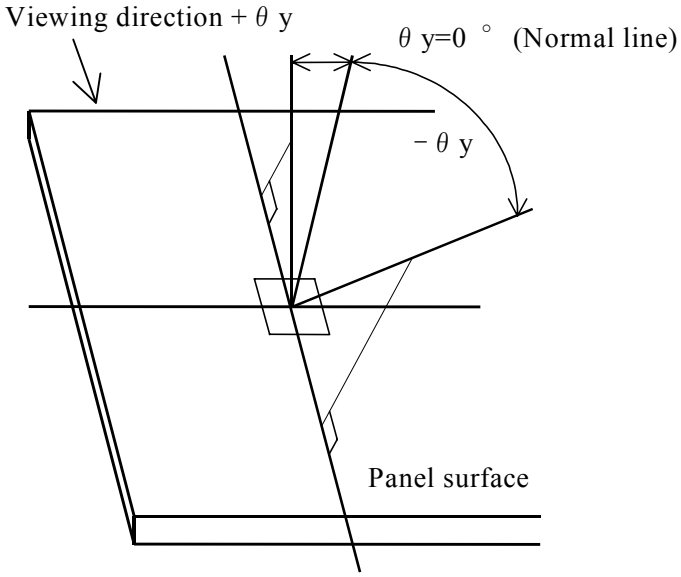


Fig.12 Definition of viewing angle

2) This module should be installed using mounting holes of metal bezel. When installing the module,pay attention and handle carefully not to allow any undue stress such as twist or bend.

3) Since the front polarizer is easily damaged. Please pay attention not to scratch on its face.
It is recommended to use a transparent acrylic resin board or other type of protective panel on the surface of the LCD module to protect the polarizer, LCD panel, etc..

4) If the surface of the LCD panel is required to be cleaned, wipe it swiftly with cotton or other soft cloth. If it is not still clear completely, blow on and wipe it.

5) Water droplets, etc. must be wiped off immediately since they may cause color changes, staining, etc., if it remained for a long time.

6) Since LCD is made of glass substrate, dropping the module or banging it against hard objects may cause cracking or fragmentation.

7) Since CMOS LSIs are equipped in this module, following countermeasures must be taken to avoid electrostatics charge.

1. Operator

Electrostatic shielding clothes shall be had because it is feared that the static electricity is electrified to human body in case that operator have a insulating garment.

2. Equipment

There is a possibility that the static electricity is charged to equipment which have a function of peeling or mechanism of friction(EX: Conveyer, soldering iron, working table), so the countermeasure (electrostatic earth:$1\times10^{8}\Omega$) should be made.

3. Floor

Floor is a important part to leak static electricity which is generated from human body or equipment.There is a possibility that the static electricity is charged to them without leakage in case of insulating floor,so the countermeasure(electrostatic earth:$1\times10^{8}\Omega$) should be made.

4. Humidity

Humidity of working room may lower electrostatics generating material's resistance and have something to prevent electrifying. So, humidity should be kept over 50% because humidity less than 50 % may

increase material's electrostatic earth resistance and it become easy to electrify.

5. Transportation/storage

The measure should be made for storage materials because there is a possibility that the static electricity,which electrify to human body or storage materials like container by friction or peeling,cause the dielectric charge.

6. Others

The laminator is attached on the surface of LCD module to prevent from scratches, fouling and dust. It should be peeled off unhurriedly with using static eliminator.

And also, static eliminator should be installed to prevent LCD module from electrifying at assembling line.

8) Don't use any materials which emit gas from epoxy resin(amines' hardener) and silicon adhesive agent(dealcohol or deoxym) to prevent change polarizer color owing to gas.

9) Since leakage current, which may be caused by routing of CCFT cables, etc., may affect the brightness of display, the inverter has to be designed taking the leakage current into consideration. Thorough evaluation of the LCD module/inverter built into its host equipment shall be conducted, therefore, to ensure the specified brightness.

10) Avoid to expose the module to the direct sun-light, strong ultraviolet light, etc. for a long time.

11) If stored at temperatures under specified storage temperature, the LC may freeze and be deteriorated. If storage temperature exceed the specified rating, the molecular orientation of the LC may change to that of a liquid, and they may not revert to their original state. Therefore, the module should be always stored at normal room temperature.

12) Disassembling the LCD module can cause permanent damage and should be strictly avoided.

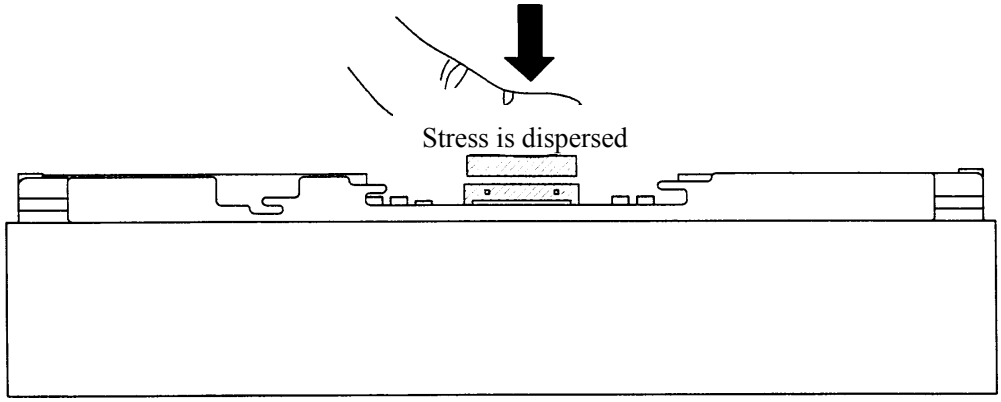
13) Procedure insert mating connector

When the mating connector is inserted, it should be parallel to the used connector of LCD module and it should be inserted on horizontal firm base.

When the mating connector is attempted to be fixed to LCD connector, it should be inserted properly in order not to create a gap as shown following diagram 2).

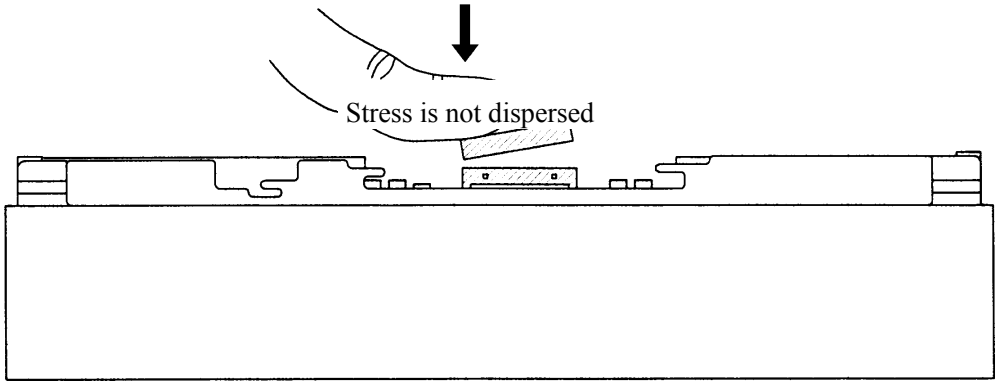
Please insert the connector as both edge is placed to the connect position of LCD connector.

1)Method of correct insert



Base (horizontal film base) is required

2) Method of wrong insert



Base (horizontal film base) is required

14) This specification describes display quality in case of no gray scale. Since display quality can be affected by gray scale methods, display quality shall be carefully evaluated for the usability of LCD module in case gray scale is displayed on the LCD module.

15) The module should be driven according to the specified ratings to avoid permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Especially the power ON/OFF sequence shown on Page 21 should be kept to avoid latch-up of drive LSI and application of DC voltage to LCD panel

16) It is a characteristic of LCD to maintain the displaying pattern when the pattern is applied for a long time.(Image retention) To prevent image retention, please do not apply the fixed pattern for along time by pre-installing such programs at your side.

17) This phenomenon (image retention) is not deterioration of LCD. If it happens, you can remove it by applying different patterns.

18) CCFT backlight should be kept OFF during VDD is "L" level.

11. Applicable inspection standard

The LCD module shall meet the following inspection standard : △1~~S-U-014~~ S-U-035

WARNING

Don't use any materials which emit following gas from epoxy resin (amines' hardener) and silicone adhesive agent (dealcohol or deoxym) to prevent change polarizer color owing to gas.

出図 ISSUE

設計通報 DRAWING INFO　連絡書 INFORMATION　No. (　)号による

新設 NEW　変更 CHANGE　書換 REPLACE　図面

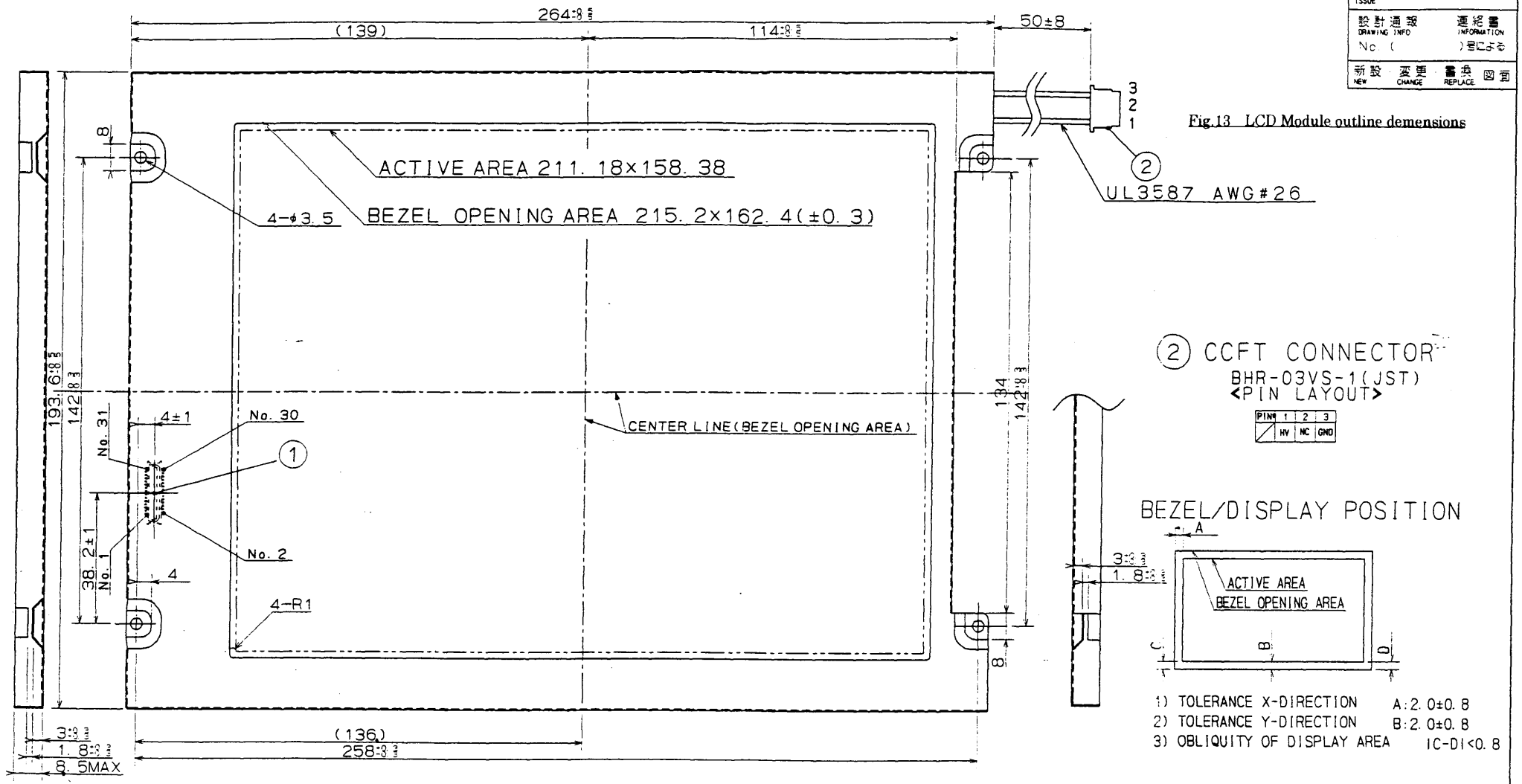


Fig.13 LCD Module outline demensions

② CCFT CONNECTOR

BHR-03VS-1(JST)

<PIN LAYOUT>

PIN	1	2	3
	HV	NC	GND

BEZEL/DISPLAY POSITION

1) TOLERANCE X-DIRECTION　A:2.0±0.8
2) TOLERANCE Y-DIRECTION　B:2.0±0.8
3) OBLIQUITY OF DISPLAY AREA　IC-DI<0.8

① INTERFACE CONNECTOR

DF98-31P-1V(HIROSE)

<PIN LAYOUT>

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	DL4	VSS	DL5	YD	DL6	LP	DL7	VSS	VSS	XCK	DL0	VCOM	DL1	VDD	VSS
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
VDD	DL2	DISP	DL3	NC	VSS	DU3	DU4	DU2	DU5	DU1	VSS	DU0	DU6	VSS	DU7

UNSPECIFIED TOLERANCE ±0.5

DATE	DIVISE	MODEL	LM10V332
MATERIAL	THICKNESS	FINISH	SCALE
NAME	LCD MODULE OUTLINE DIMENSIONS		
SYMBOL	640xRGBx480 P0.33		
PARTS CODE			
DESIGN	CHECK	APPROVE	SHARP CORPORATION
城山			シャープ株式会社 液晶奈良(事本)
			先行部門 アコーディー開発センター第1技術部
DATE	1999・2・17・		
DRAWING No.	ODI0V3321110		

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